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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,478	07/14/2004	Thomas L. McDevitt	BUR920040059US1	4477
30449	7590	09/25/2006	EXAMINER	
SCHMEISER, OLSEN & WATTS 22 CENTURY HILL DRIVE SUITE 302 LATHAM, NY 12110			ULLAH, ELIAS	
			ART UNIT	PAPER NUMBER
			2812	

DATE MAILED: 09/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/710,478	Applicant(s) MCDEVITT ET AL.	
	Examiner Elias Ullah	Art Unit 2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 July 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 13-32 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 13-32 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 July 2004 is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>8/9/2004, 7/14/2004</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This office action in response to Election Restriction requirement filed on 7/26/2006.

Election/Restrictions

1. Applicant's election with traverse of group II in the reply filed on 7/26/2006 is acknowledged. The traversal is on the ground(s) that the different groups of invention do not place a serious burden upon the examiner. This is not found persuasive because the examiner respectfully submits that the different groups are searched in different areas and therefore examining both groups would place a serious burden upon the examiner.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 13-16, and 23-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Huang et al.

3. As to claim 13, Huang et al shows a method of fabricating a dual damascene structure, comprising: forming a first interconnect level comprising a first dielectric layer and including a multiplicity of first damascene or dual damascene conductive wires, each first damascene or dual damascene conductive wire extending from a top surface

of said first dielectric layer a distance toward a bottom surface of said first dielectric layer, said distance less than a thickness of said first dielectric layer (col. 6, line 8-35, Fig. 5a-5c); forming a second interconnect level directly above and in contact with said first dielectric layer, said second interconnect level comprising a second dielectric layer and including a multiplicity of second dual damascene conductive wires, each second dual damascene conductive wire extending from a top surface of said second dielectric layer a distance toward a bottom surface of said second dielectric layer, said distance less than a thickness of said second dielectric layer; and forming a dual damascene conductive via bar within said second interconnect level and integral with and extending from a bottom surface of one of said multiplicity of said second dual damascene conductive wires and a top surface of one of said multiplicity of said first dual damascene conductive wires, said dual damascene conductive via bar having a length greater than its width, said length and width of said dual damascene conductive via bar extending in said plane defined by said top surface of said second dielectric layer (Col. 6, lines 8-37, Fig. 5a-5c).

4. As to claim 14, Huang et al shows the method of claim 13, further including: forming a dual damascene conductive via within said second interconnect level and integral with and extending from a bottom surface of one of said multiplicity of said second dual damascene conductive wires and a top surface of one of said multiplicity of said first dual damascene conductive wires, said dual damascene conductive via having a length about equal to its width, said length and width of said dual damascene

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conductive via extending in a plane defined by said top surface of said second dielectric layer (Fig. 5a, 5c, col. 6, lines 8-37).

5. As to claims 15-16, Huang et al shows the method of claim 13, further including: forming an additional conductive dual damascene via bar within said first interconnect level, said additional conductive via bar extending from a bottom surface of one of said multiplicity of said second dual damascene conductive wires a distance toward said bottom surface of said first dielectric layer, said distance less than a distance between said additional conductive dual damascene via bar and said bottom surface of said first dielectric layer; the method of claim 13, further including: forming an additional conductive dual damascene via bar within said first interconnect level, said additional conductive via bar extending from said top surface of said first dielectric layer a distance toward said bottom surface of said first dielectric layer, said distance less than said thickness of said first dielectric layer (Fig. 5a, 5c, col. 6, lines 8-37).

6. As to claims 23-24, Huang et al shows wherein said dual damascene conductive wires and said dual damascene conductive via and said dual damascene via bar comprise a same conductor selected from the group consisting of copper, tungsten, aluminum, aluminum-copper alloy, polysilicon, tantalum, tantalum nitride, tantalum silicon nitride, titanium, titanium nitride, titanium silicon nitride, tungsten, tungsten nitride, tungsten silicon nitride and combinations thereof; wherein said dielectric layer is selected from the group consisting of silicon oxide, $\text{SiC}_x\text{O}_y\text{H}_z$ and poly(arylene) ether (col. 8, lines 20-27).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claim 25-26, 30-32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. in view of Adams et al.

9. As to claims 25-26, Huang et al. shows a method of fabricating a dual damascene structure, comprising: providing a substrate; forming a dielectric layer on said top surface of said dielectric layer; forming a via bar opening in said dielectric layer, said via bar opening having a length greater than its width, said length and width of said via bar opening extending in said plane defined by said top surface of and dielectric layer, said via bar opening extending through the entire thickness of said dielectric layer; etching a first trench in said dielectric layer, said first trench aligned to said via bar opening, said first trench extending from said top surface of said dielectric layer toward a bottom surface of said dielectric layer a distance less than a thickness of said dielectric layer (col. 6, lines 8-37, Fig. 5a-5c), but Huang et al fails to disclosed applying an anti-reflective coating to a top surface of said dielectric layer, said antireflective coating filling said via bar opening; applying a masking layer to a top surface of said anti-reflective coating; etching said antireflective coating from said via bar opening and forming a first trench in said dielectric layer over said via bar opening, removing said masking layer and any remaining antireflective coating.

10. As to claims 25-26, Adams et al. teaches applying an anti-reflective coating to a top surface of said dielectric layer, said antireflective coating filling said via bar opening; applying a masking layer to a top surface of said anti-reflective coating; etching said antireflective coating from said via bar opening and forming a first trench in said dielectric layer over said via bar opening, removing said masking layer and any remaining antireflective coating (col. 7, lines 43-63).). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to add ARC to lithography process of Huang et al. lithography process because such a process is used to damascene wire pattern.

11. As to claims 30-32, Huang et al shows wherein said dual damascene conductive wires and said dual damascene conductive via and said dual damascene via bar comprise a same conductor selected from the group consisting of copper, tungsten, aluminum, aluminum-copper alloy, polysilicon, tantalum, tantalum nitride, tantalum silicon nitride, titanium, titanium nitride, titanium silicon nitride, tungsten, tungsten nitride, tungsten silicon nitride and combinations thereof; wherein said dielectric layer is selected from the group consisting of silicon oxide, $\text{SiC}_x\text{O}_y\text{H}_z$ and poly(arylene) ether (col. 8, lines 20-27).

1. As to claim 31, differences in processing range of 400 nm to about 800 nm will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "Where there general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454,

456, 105 USPQ 233, 235 (CCPA 1955). Furthermore, it would have obvious to one of ordinary skill in the art at the time of invention was made to determine through routine experimentation the optimum based upon a variety of factors wherein said anti-reflective coating has a thickness of between about 400 nm to about 800 nm, such limitation would not lend patentability to the instant application absent a showing of unexpected results.

Allowable Subject Matter

12. Claims 17-18, 27-29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following subject matters are allowable "first dielectric layer includes a first dielectric diffusion barrier layer, a bottom surface of said first dielectric diffusion barrier layer being co-extensive with said bottom surface of said first dielectric layer and said second dielectric layer includes a second dielectric diffusion barrier layer, a bottom surface of said second dielectric diffusion barrier layer being co-extensive with said bottom surface of said second dielectric layer".

Claims 19-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following subject matters are allowable "forming a spiral shaped dual damascene conductive via bar in said first dielectric layer, forming a spiral shaped dual damascene conductive via bar in said second dielectric layer; or

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forming spiral shaped dual damascene conductive via bars in both said first and said second dielectric layers, top edges of said spiral shaped dual damascene conductive via bars co-planer with top surfaces of corresponding dielectric layers and bottoms edged of said spiral shaped dual damascene conductive via bars co-planer with bottom surfaces of said corresponding dielectric layers and sidewalls of said spiral shaped dual damascene conductive via bars aligned to one another and stacked in electrical contact on top of one another”.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elias Ullah whose telephone number is 571-272-1415. The examiner can normally be reached on 8-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, MICHAEL LEBENTRITT can be reached on (571)272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

E. Ullah.
September 13, 2006.


MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER